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Harmonic Analysis and Design of LC Filter for a Seven-level Asymmetric Cascaded Half Bridge Multilevel Inverter

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***Abstract*—As a lot of multilevel inverter designs are being introduced in order to generate an output voltage that resembles a pure sinusoidal waveform, a need is felt for balancing the number of output voltage levels with the amount of static switches required for a sustainable development. Many optimal topologies have been suggested, as of now, that seem to have resulted in the reduction of number of switches required to generate a certain number of level in the output. Carrying the same ideology forward, this paper illustrates a half-bridge inverter being operated on two PWM switching strategies followed by designing of a suitable passive harmonic LC filter for an improved power quality output. The modification thus suggested, has also been justified with simulation results.**

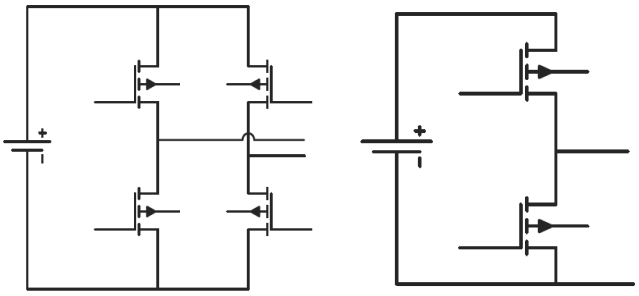
***Index Terms*—Modulation index (MI), Multilevel inverter (MLI), Power quality, Switch-count, Total harmonic distortion (THD).**

I. INTRODUCTION

The use of static switches has enabled endless possibilities for designing a wide range of multilevel inverters with a much more improved power quality response. The quality of output voltage waveform has been shown to be related to the number of staircase levels in output waveform, and also, to the switch-count of the corresponding inverter arrangement [1-3]. For this very reason, a variety of discrete MLI arrangements have been in use till now that include Neutral Point Clamped, Flying Capacitor and Cascaded H Bridge [4-6]. Among all other inverter configurations, cascaded H Bridge has achieved a limelight from the researchers for its reasonable simplicity, compact control circuit designs and reduced switch-count requirement [7, 8].
To follow up, MLIs from the CHB topologies can be differentiated on the basis of the dc voltage sources being used. For a symmetric model, dc sources in all cascaded sections will have equal magnitudes.

On the other hand, an asymmetric inverter will have different dc sources in all cascaded cells providing more flexible operation. The later has been proven to generate more staircase levels in output while using same amount of dc sources as in symmetrical configuration.

This added advantage of asymmetrical cascaded MLI is highlighted throughout the discussion in this paper as well. The basic structure of a cascaded H bridge inverter is shown in Fig. 1.



(a) (b)

Fig. 1. Configuration of H bridge Inverter (a) Full Bridge, (b) Half bridge.

II. ASYMMETRIC CASCADED HALF BRIDGE ARRANGEMENT

The use of half bridge is even more beneficial as it reduces the need of using four switches in each cell. Instead, only a couple of switches are required to serve the purpose. The general outlook of a half H bridge asymmetric MLI is shown in Fig. 2. Every cell has a different dc source value. For the selection of dc sources and an equally stepped output, binary method has been used which states that the magnitude of the succeeding dc source should be twice the magnitude of the preceding one as governed by (2).

For *n* cells, having a single source per cell, dc source values can be selected from cell '1' to '*n* – 1' as described by (1) and (2).

$$Vdc_1 = Vdc \quad (1)$$

$$Vdc_{(n-2)} = 2\ Vdc_{(n-1)} \quad (2)$$

The magnitude of the last dc source Vdc_n will be the sum of all other dc sources as described by (3).

$$Vdc_n = \sum_{i=1}^{n-1} Vdc_i \quad (3)$$

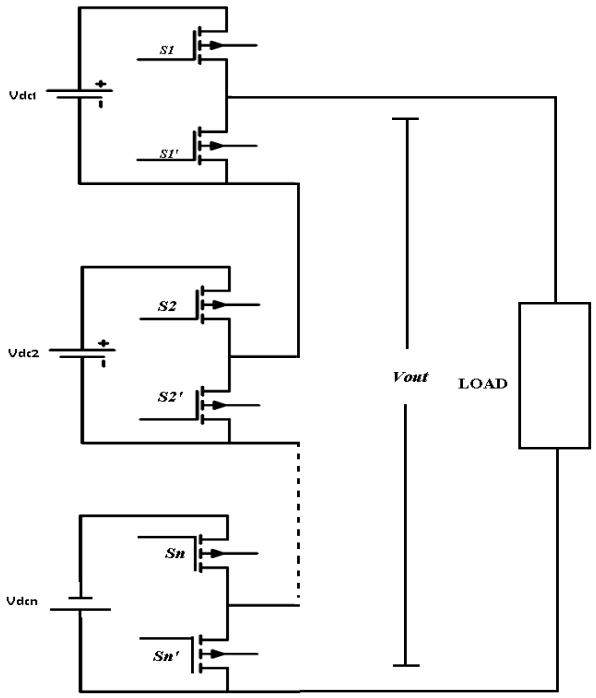


Fig. 2. Asymmetric cascaded inverter with *n* cells.

It is worth mentioning that the last source is connected in reverse polarity as it is used to generate the negative half cycle of the waveform. In addition, the value of this last dc source will be the same as that of the peak output voltage V_{MAX}. Every cell is equipped with two switches S_n and S_n'. Both of them work in a complementary manner. Switch S_n is used to connect the corresponding dc source to the load. In contrast, turning on S_n' disconnects the corresponding source from the load. The output voltage will have number of levels that are governed by (4) as,

$$N_{level} = 2^{n-1} \quad (4)$$

Whereas, the total number of switches N_{SW} required in terms of the dc sources used is given by (5) as,

$$N_{SW} = 2n \quad (5)$$

For simulation purposes, a three-cell design is being discussed here. In this case, the switching pattern to be followed is shown in Table I. The 1's denote ON state while 0's denote OFF state of switches. Turning on S_1 gives a *+Vdc* output. Similarly, by switching on S_2, we can get *+2Vdc* at the output. On the other hand, triggering S3 will result in a voltage of *-3Vdc* at the output. Hence, with the help of proper switching, a seven-level output voltage is achieved [1]. The resulting output voltage is shown in Fig. 3.

Table I. Switching sequence of S_1, S_2 and S_3.

State	S_1	S_2	S_3	V_{out}
1	0	0	0	0
	1	1	1	--
2	1	0	0	V_{dc}
3	0	1	0	$2V_{dc}$
4	1	1	0	$3V_{dc}$
5	0	1	1	$-V_{dc}$
6	1	0	1	$-2V_{dc}$
7	0	0	1	$-3V_{dc}$

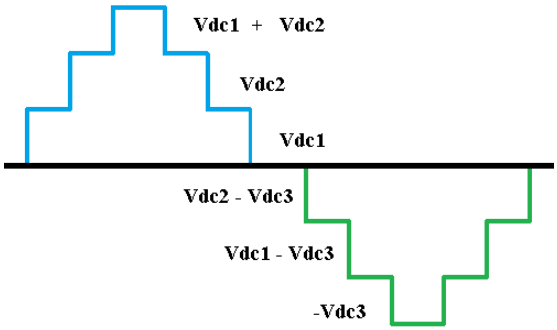


Fig. 3. Seven level output voltage.

III. SWITCHING STRATEGIES

For this topology, at higher switching frequencies, PWM switching strategies provide a better and more suitable result [1]. Many different techniques like Conventional PWM, Sinusoidal PWM, Space vector PWM, Sub harmonic PWM, Phase shifted PWM and Multicarrier PWM, have been in used for quite a while [8-12]. In this paper, two of the different multicarrier PWM strategies namely, Phase Opposition Disposition PWM and Alternate Phase Opposition Disposition PWM, have been utilized for analysis of inverter harmonic response.

A. Phase Opposition Disposition PWM

In phase opposition disposition PWM, the carriers above zero level are in phase. While, those below the zero level, are out of phase as shown in Fig. 4. Having six swtiches in total, six carrier signals are used for generating control signals for all of the switches. At all those points where the carrier singals intersect with the reference sine wave, a pulse is generated which is sent towards the gates of corresponding switches.

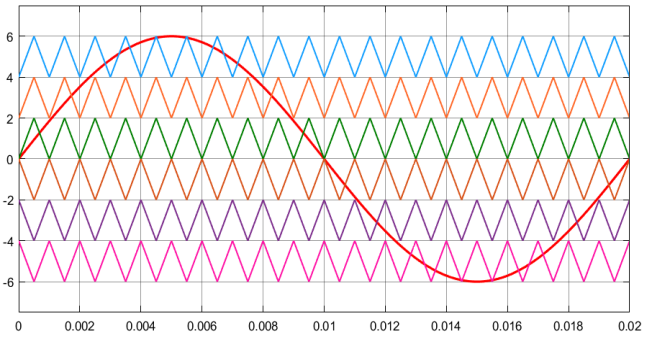


Fig. 4. Six carrier signals for Phase disposition PWM.

B. *Alternate Phase Opposition Disposition PWM*

In this strategy, every alternate carrier is out of phase as shown in Fig. 5.

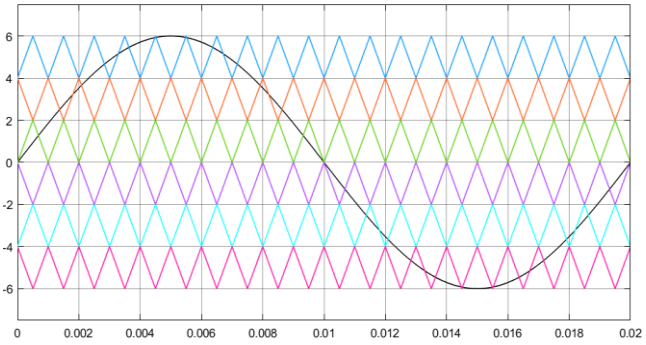


Fig. 5. Six carrier signals for Alternate phase opposition disposition PWM.

IV. DESIGN OF A LC LOW PASS FILTER FOR HARMONIC MITIGATION

In order to reduce the harmonic contents of output voltage, a passive LC filter is designed. At first, few different filter configurations were considered. The basic form of LC filter is an *L-Network* as shown in Fig. 6(a). However, for a sharper response, a Pi-Network can also be considered as shown in Fig. 6(b). For an even sharper output, a combination of both networks can be adopted. It is then, termed as a *Pi – L* Network as shown in Fig. 6(c).

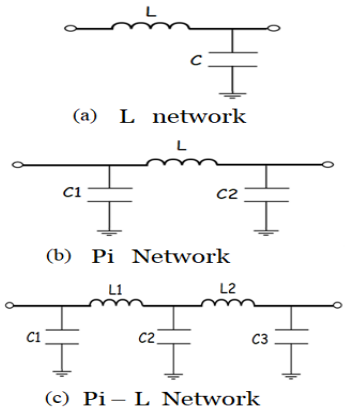


Fig. 6. LC Filter Configurations

For this inverter, a *Pi – L* network is chosen given its sharpest acting response as shown in Fig. 7. The basic ideology in all of these configurations is that the inductance L blocks the high frequency components present in the output of inverter. On the other hand, the capacitance C provides an easy path for such higher frequency elements towards the ground.

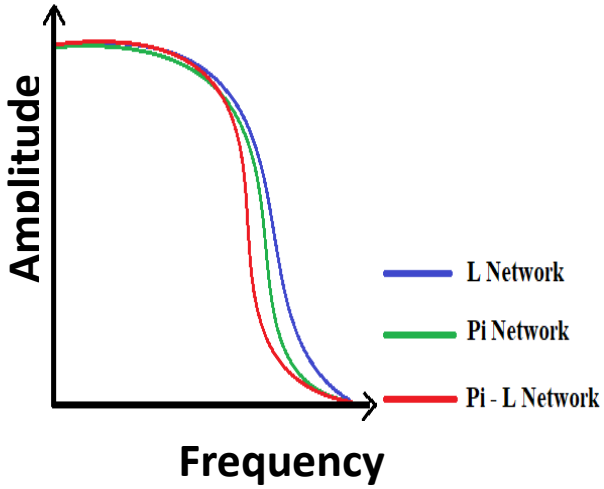


Fig. 7. Response comparison for three different LC filter configurations.

For calculation purposes, the values for peak output voltage V_{MAX} is selected depending upon the selection of dc sources. Also the required output voltage magnitude is considered. Then, the switching frequency f_{SW} is set. After which, the value of cut off frequency f_C can be known by (6). In the end, for determining the values of inductance L and capacitance C, (7) and (8) are used respectively.

$$f_c = 10\% \ of \ f_{SW} \tag{6}$$

$$L = \frac{0.03 \ V_{MAX}}{2 \pi f I_{L\,max}} \tag{7}$$

$$C = \frac{1}{(2 \pi f_C)^2 \ L} \tag{8}$$

V. SIMULATION

The simulation of this type of inverter is performed in *Simulink* MATLAB r2018a as shown in Fig. 8. The key specifications set for the inverter are listed in Table II.

A. *Without Inclusion of LC Filter*

For simulation of inverter without using any LC filter, the simulation model shown in Fig. 8 is compiled. The inverter is run with a modulation index (MI) which is given as a ratio of magnitude of modulating signal (Ma) to the magnitude of carrier signal (Ac) as described in (9).

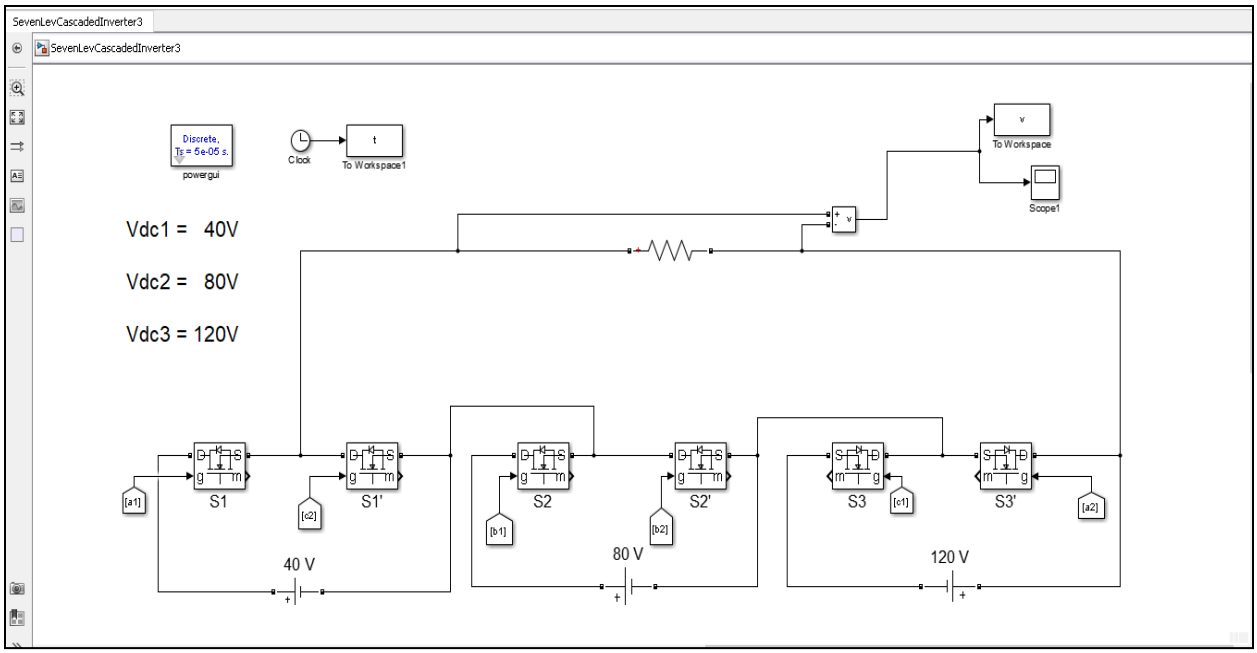


Fig. 8. Simulation Model for Seven-level Asymmetric Inverter without LC filter.

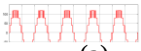
Table II. Simulation parameters

Number of dc sources	**03**
Number of switches	**06**
Types of switches	**MOSFET**
Vdc1	**40 V**
Vdc2	**80 V**
Vdc3	**120 V**
Peak Output Voltage V_{max}	**120 V**
Load	**720 W**
Filter Inductance L	**6 mH**
Filter Capacitance C	**0.2 µF**

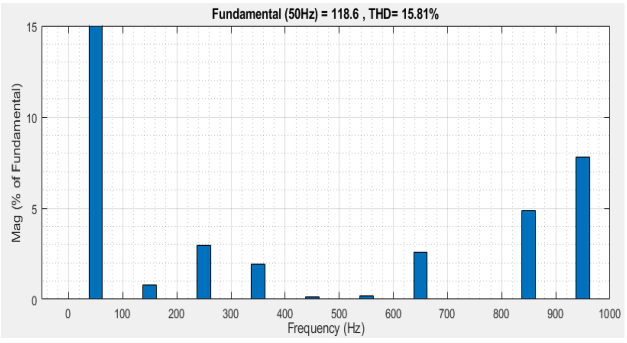
$$MI = \frac{Ma}{3\,Ac} \quad (9)$$

Taking the amplitude of modulating signal as 6 units and that of carriers as 2 units, the modulation index becomes 100%. With phase opposition disposition PWM strategy being used for switching of MOSFET switches, the output voltage waveform thus obtained, is shown in Fig. 9(a) along with its FFT response showing a total harmonic distortion of 15.8% as indicated in Fig. 9(b).

When alternate phase opposition disposition PWM technique is used, the output voltage thus obtained, is shown in Fig. 10(a) along with its FFT analysis shown in Fig. 10(b). In this case, THD comes out as 18.7%.



(a)



(b)

Fig. 9. Output voltage response on POD-PWM without LC filter.

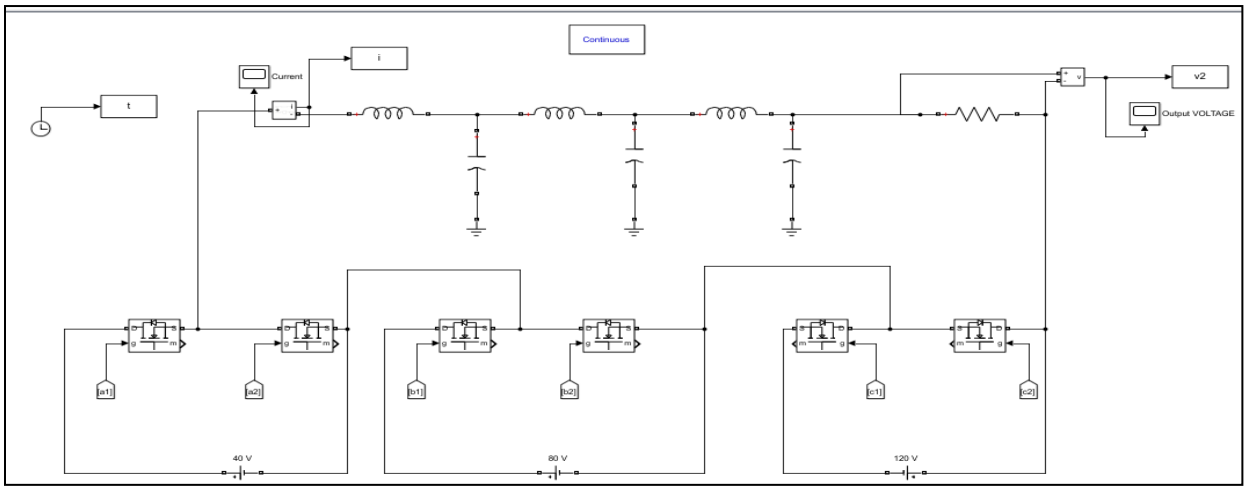
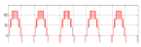
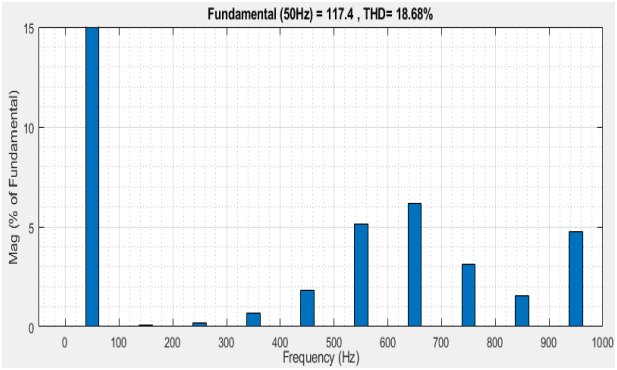


Fig. 11. Simulation Model for Seven-level Asymmetric Inverter with LC filter.



(a)

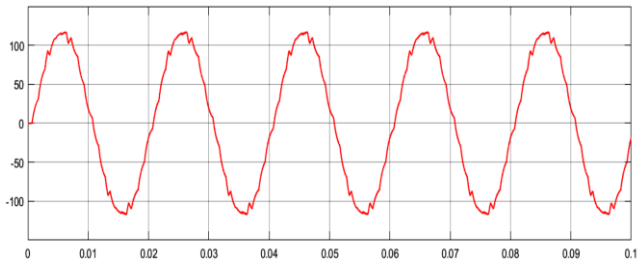


(b)

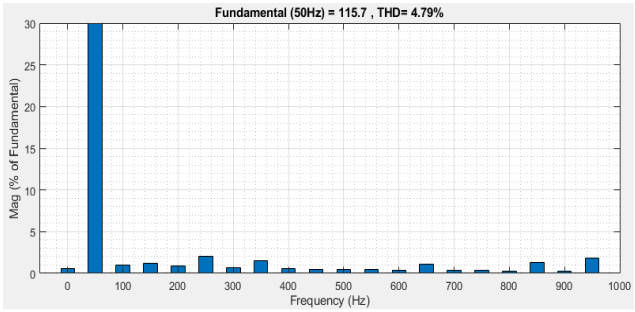
Fig. 10. Output voltage response on APOD-PWM without LC filter.

B. *With Inclusion of LC Filter*

The previously designed LC filter is now included in the simulation model of inverter as shown in Fig. 11. All the other parameters of the Simulink model are maintained ate previous values. When the simulation is performed using POD-PWM technique, the resulting output voltage is shown in Fig. 12(a) alongwith its FFT analysis in Fig. 12(b).



(a)



(b)

Fig. 12. Output voltage response on POD-PWM with LC filter

Fig. 13(a) shows the output voltage of inverter when run with APOD-PWM switching technique along with the FFT response shown in Fig. 13(b).

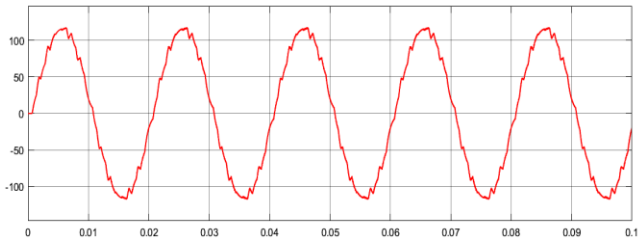


Fig. 13(a). Output voltage response on APOD-PWM with LC filter

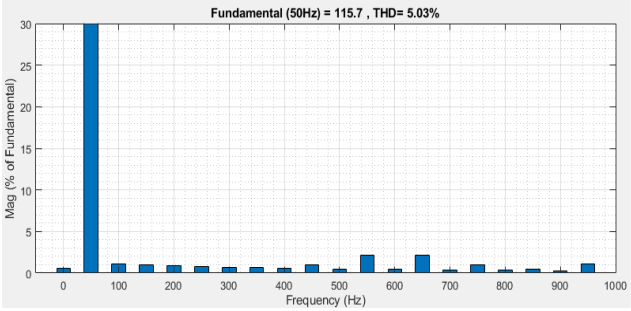


Fig. 13(b). Output voltage response on APOD-PWM with LC filter

VI. COMPARISON AND RESULTS

For suggesting a better switching technique among the two which are observed in this paper, following results need to be observed as pointed out in Table III.

Table III. Simulation Results showing THD values before and after application of LC filter.

Conditions	*THD at POD-PWM (%)*	*THD at APOD-PWM (%)*
Without LC Filter	***15.81***	***18.68***
With LC Filter	***4.79***	***5.03***

By observing Table III, it is obvious that the first switching technique namely, phase opposition disposition PWM, has proven to give a better power quality in the output voltage waveform as compared to the latter even without the application of the designed harmonic filter. Furthermore, filter application mitigates an appreciable amount of harmonic content from the output and has brought down the THD values below 5% which counts to about 70% reduction in total harmonic distortion.

VII. CONCLUSION

Asymmetric cascaded inverters can not only provide the much needed simplicity in the designs of control circuits but the reduction in the overall cost as well due to their requirement of less number of power electronic switches for generating more staircase levels in output waveform. These inverters can be operated with different PWM switching strategies like the ones illustrated in this paper and can be optimized by the use of specifically designed harmonic filter as discussed before. The performance of inverter becomes quite satisfactory when LC filter is applied at its output.

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