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Simulation and Analysis of Multicarrier PWM Techniques for Reduced Device Count Multilevel Inverter.

[a*] Sawira Bhatti.
Mehran University of Engineering and Technology Jamshoro, Sindh, Pakistan
Corresponding author e-mail: (Sawerak251@gmail.com)
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Abstract: **In this developing period, a trend is Multilevel inverters due to the advancement in power conversion technology. Multilevel inverters provide multi stepped output levels that is better than two or three level inverters. By increasing the voltage levels, number of semiconductor devices and DC sources are also increase. To overcome this drawback of MLI, the reduced device count topologies are used. The asymmetrical DC voltage sources are used in reduced device count multilevel inverter to get the desired 7 voltage levels. The multicarrier PWM techniques are used to reduce the switching losses and generate switching signals for RDC MLI. The multicarrier PWM techniques are utilized in RDC MLI to get effective output voltage with less harmonics. The focus of this paper to implement and analyze the level-shifted POD and APOD multicarrier pulse- width modulation technique in reduced device count CHB Multilevel inverter. The circuit is simulated and analyzed by MATLAB software. The alternate phase opposition disposition (APOD) MCPWM has less THD than phase opposition disposition (POD) MCPWM. Therefore, the APOD MCPWM has better performance in reduced device count multilevel inverter.**

***Index Terms*— Reduced Device Count Multilevel Inverter, Multicarrier PWM, Total Harmonic Distortion¸ Asymmetrical.**

I. INTRODUCTION

Power converters have become a fundamental factor of today's ultra-modern world. Multilevel inverter (MLI) is predominant to conventional two-level inverter, as it produces multi stepped output voltage waveform approximated to sinusoidal. Multilevel inverters are superiority in high power high voltage applications due to better harmonics spectrum, high switching frequency, reduced size, low dv/dt, High efficiency [1]. They have been widely applied in multiple applications such as uninterruptable power supplies (UPS), micro grids, motor drivers, flexible AC transmission systems, photovoltaic applications [2].

The conventional topologies of multilevel inverters are diode-clamped multilevel inverters (DC-MLI), flying capacitor multi-level inverters (FC-MLI), and cascaded H-bridge multilevel inverters (CHB-MLI). The CHB-MLI is most admired and widely used in many applications. The configuration of this CHBMLI is simpler and required less components then DCMLI and FCMLI. It consists of semiconductor devices and DC sources whose quantity depend on the output voltage levels. Each bridge contains one 4 switches with one DC source [3][4]. CHBMLI is further classified as symmetric and Asymmetric multilevel inverters. When each bridge Contain uniform DC voltage source then it is known as symmetrical MLI, if both are not identical, is called Asymmetrical MLI [5]. Multilevel inverters are needed more components count to increase the voltage levels. Which may cause to increase the complexity in designing, make system bulky and more costly. So, for get over these problems the reduced device count (RDC) multi-level inverter topology is used [6]. The PWM techniques are utilized for the purpose of switching control in CHB multilevel inverters [7]. There are some modulation strategies are used to generate output voltage of RDC MLI. Few are categorized as Square wave PWM, hysteresis controller, space vector, carrier PWM. Different MCPWM techniques are used such as level-shifted Phase disposition, Phase opposition disposition, Alternate phase opposition disposition and many others for improving the power quality [8]. Harmonic is component with integral multiple of fundamental frequency. Any waveform except sinusoidal consist of harmonics. Complex waveforms contain different frequency, harmonics, and amplitude which are out of phase with each other [9]. Multicarrier PWM techniques applied to decrease THD of output. Increase in switching frequency caused to decrease THD. Harmonic reduction by these techniques will directly affect the performance of multilevel inverter [10].

With main motive of improving the output voltage waveform with less complexity of system, reduced device count multilevel inverter is implemented through various control switching strategies of multicarrier PWM. The objective of paper is to analyze the most effective multicarrier PWM technique to reduce the THD in RDC MLIs. The research highlights the best technique by using MATLAB/Simulink in reduced device count multilevel inverter by implementing multicarrier PWM techniques, level-shifted POD and level-shifted APOD to get the Seven-level RDC MLI with asymmetrical DC voltage sources.

II. METHODLOGY

A. Operation principle of reduced device count CHB MLI.

The reduced device count multi-level inverters produces a smooth multi stepped output voltage waveform with smaller number of semiconductor switches and DC source. Circuit consists separate part of polarity and level generation. Fig.1 shows experimental circuit of RDC MLI. It contains 8 IGBT

semiconductor switches with two asymmetrical DC sources are used to produce the 7-voltage levels. As shown in figure, switches S1, S2, S3, and S4 used for polarity generation and level is generated by switches S5, S6, S7, and S8. The S1 and d S2 conduct during positive cycle while S3 and S4 conduct during negative cycle of output voltage.

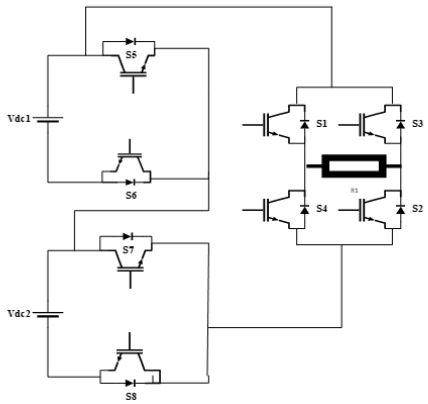


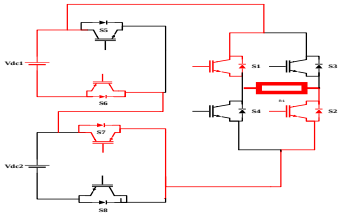
Fig. 1. Proposed topology of RDC-MLI

In fig.2, the operating modes of given RDCMLI are shown. Red color indicates the conduction of switches while black color shows the off state of switches. 7-level RDC-MLI generate three positive, three negative and one zero voltage level. The switching table of switches is given in Table I.

TABLE I: Switching Table.

Levels	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
+V	On	On	Off	Off	Off	On	On	Off
+2V	On	On	Off	Off	On	Off	Off	On
+3V	On	On	Off	Off	Off	On	Off	On
0	On	On	Off	Off	Off	Off	Off	Off
-V	Off	Off	On	On	Off	On	On	Off
-2V	Off	Off	On	On	On	Off	Off	On
-3V	Off	Off	On	On	Off	On	Off	On

B. Operating Modes



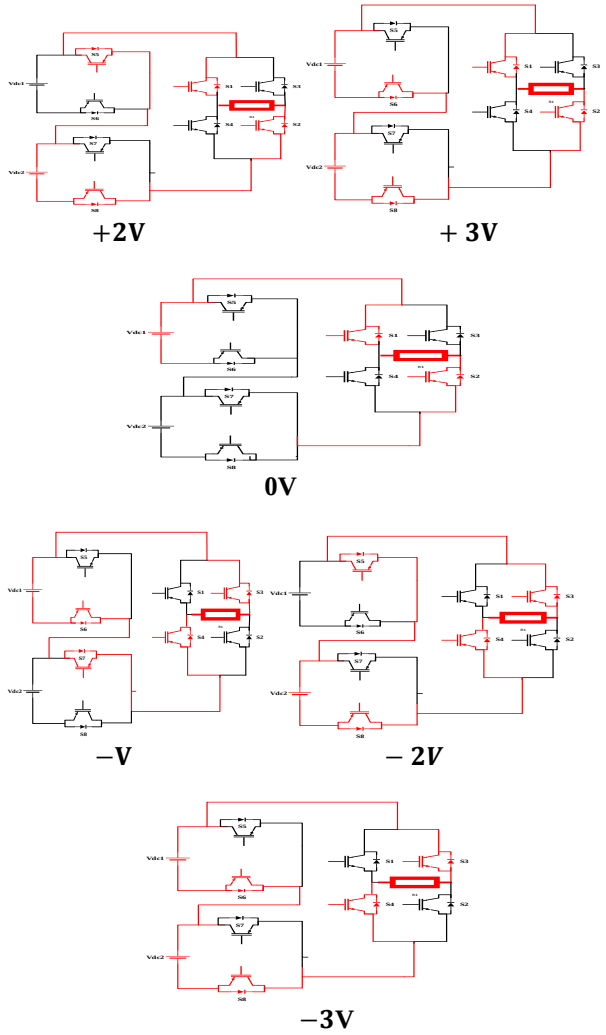
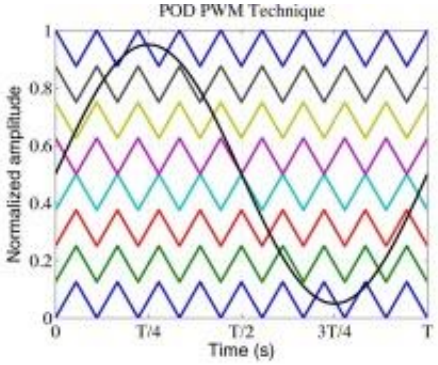


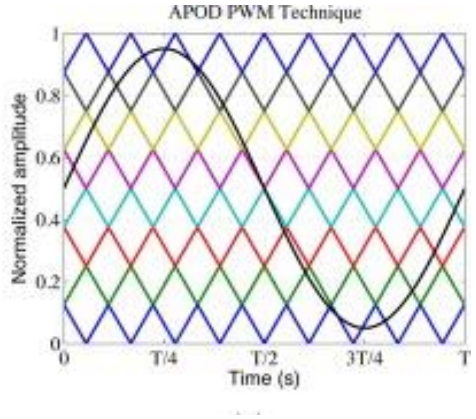
Fig.2. Operating modes of proposed RDC-MLI

C. MULTICARRIER LEVEL-SHIFTED PWM TECHNIQUES

The PWM techniques are the most effectual way of switching control for multi-level inverters. These techniques are implemented to get the desired output of RDCMLI. The multiple triangular waves of high frequency are generated then they are compared to reference sine wave. The proposed 7-level reduced device count multilevel inverter is implemented by the POD MCPWM and APOD MCPWM techniques with 6 carrier waveforms of pulse-width modulation. In POD, carrier wave above the x-axis has 180° phase shift compared to carrier below the x-axis. In APOD, each carrier has 180° phase shift to each other.



(a)



(b)

Fig.3. Waveform of (a) Phase opposition disposition MCPWM, (b) Alternate phase opposition disposition MCPWM

III. Simulation

The proposed 7-level RDC-MLI is simulated by using MATLAB/Simulink software. Simulation consists one part of inverter circuit and other part of control circuit for switching of IGBTs. The control circuit contain logic gates, which are arranged as the polarity generation switches S1, S2, S3, S4 generate polarity. S1, S2 conduct during positive cycle, while S3, S4 are used in negative cycle of output.

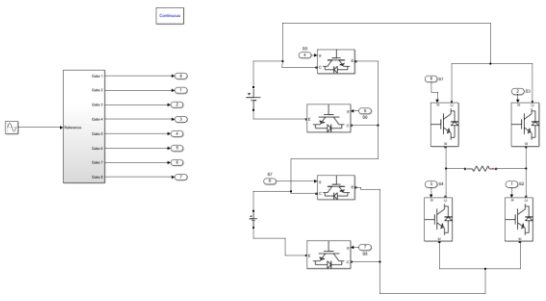


Fig.3. Simulation circuit of proposed RDC-MLI.

The RDC MLI circuit contains 8 IGBTs with two DC voltage sources. DC sources are asymmetrical, value of Vdc1 is 104V and Vdc2 has 208V. Logic gates are used to trigger the IGBTs in reduced device count multilevel inverter with 6 high frequency triangular carrier signals and reference sinusoidal wave. Zero-carrier is applied to switches S1 and S2 and opposite will be applied to the S3 and S4. The switches S5, S6, S7, S8 should not be trigger at the same time therefore proper combination of logic gates are used in proposed RDC-MLI.

TABLE II. Parameters of Simulation Model

No: Of IGBTs	8
DC sources	2
Output voltage levels	7
Carrier signals	6
Resistive load	100 ohms
Frequency of sine waveform	1.5kHz

IV. Result and Discussions

MATLAB/Simulink is used to simulate the reduced device count multilevel inverter. The Phase opposition disposition MCPWM and Alternate phase opposition disposition MCPWM techniques are applied to reduced device count multi-level inverter. The focus of the paper is to analysis harmonics in output voltage of proposed RDC-MLI with these POD and APOD multicarrier PWM techniques. The proposed RDC-MLI is better than conventional as it required a smaller number of semiconductor devices (IGBTs) and DC voltage source compared to traditional MLIs. The reduced device count topology decreases the complexity, cost of the system with less harmonic distortion by using MCPWM techniques.

The phase opposition disposition PWM technique with 6 carrier signals to get the 7-levels of output voltage. In POD MCPWM, all carrier above X-axis is 180° phase shifted to the carriers below the X-axis. The waveform of implemented Alternate phase opposition disposition MCPWM technique is shown in figure. 4.

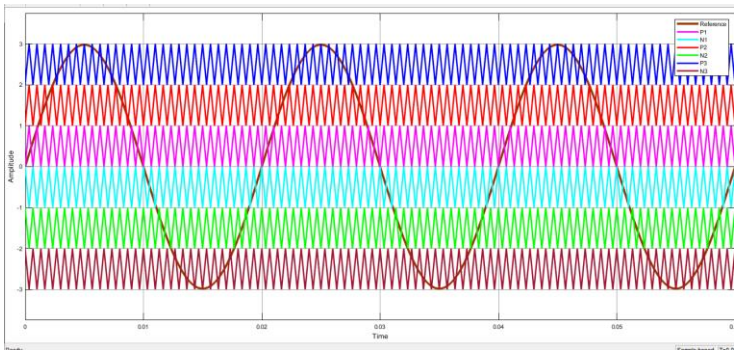
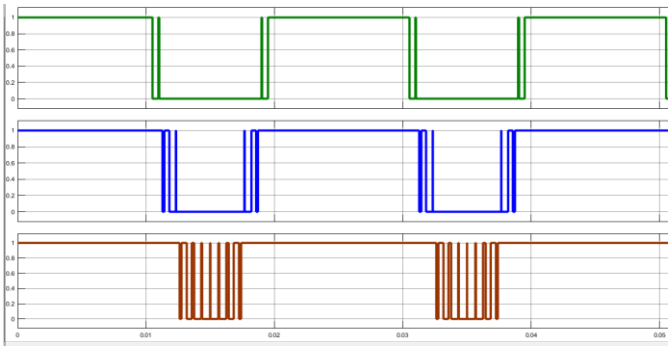
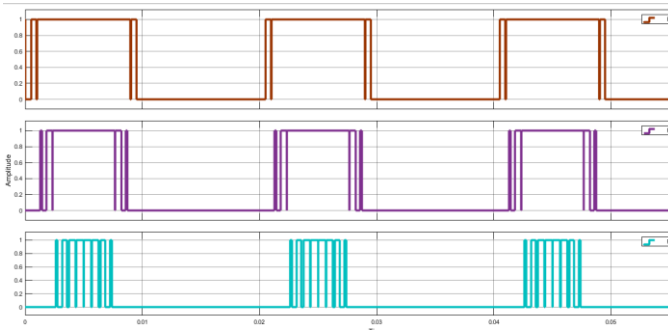


Fig.4. Phase opposition disposition MCPWM.

The Carrier signals are given to relational operator, then to logic gates and the combination of logic gates send to the IGBTs of RDC-MLI. The 3 positive (P_1, P_2, P_3) and 3 negative (N_1, N_2, N_3) carrier signals of relational operators of POD MCPWM are shown in fig 5 (a) and (b).

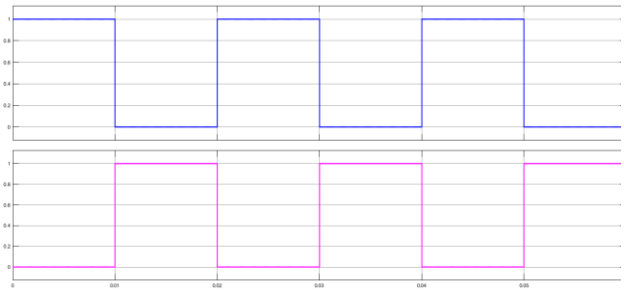


(a)



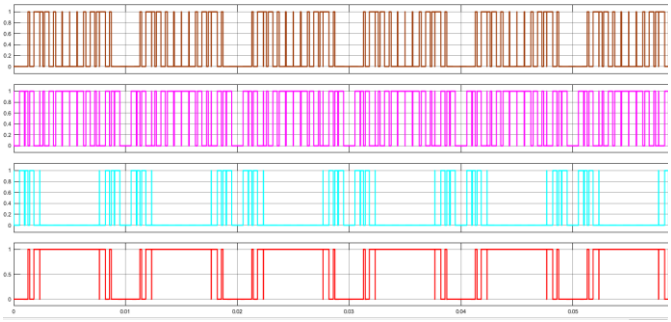
(b)

The polarity generation switches conduct for 20 milli seconds with respective 50 Hz frequency. The S1, S2 conduct for 10 msec each for positive half cycle while S3, S4 are negative cycle of output voltage. The pulse for S1, S2 are shown in fig.5 (c).



(c)

The switches S5, S6, S7, S8 are conduct for level generation. Pulses of these switches are shown in fig.5 (d).



(d)

Fig.5. Control signals of POD MCPWM

(a)N_1, N_2, N_3, (b)P_1, P_2, P_3, (c)S_1, S_2, S_3, S_4, (d) pulses for S_5, S_6, S_7, S_8.

The 7-levels Output voltage waveform of RDC Cascaded H-bridge MLI implemented by POD MCPWM technique contain three positive, three negative and a zero voltage levels.

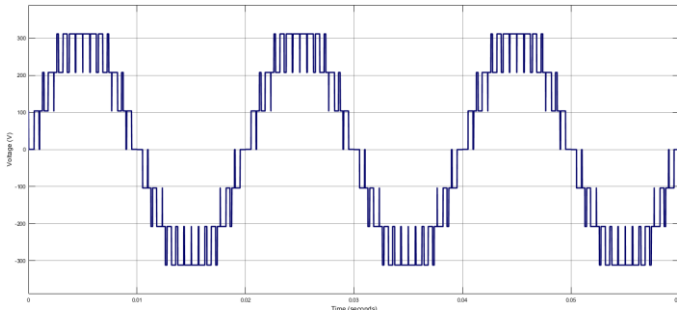


Fig.6. Output voltage waveform of proposed RDC-MLI implemented by POD MCPWM.

The waveform of phase opposition disposition MCPWM technique is shown in fig.7. Six carrier signals are applied to get the 7-levels of voltage at output of RDC-MLI. Each carrier below and above the X-axis are phase shifted by 180° to each other.

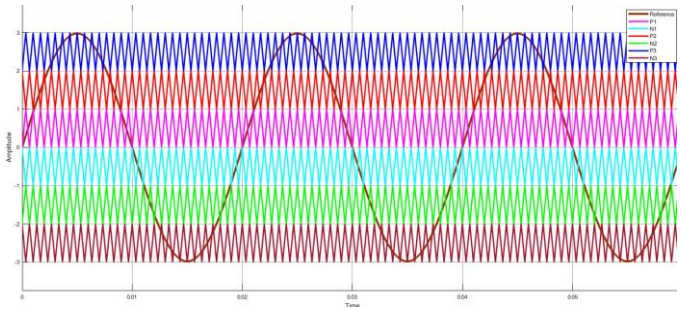
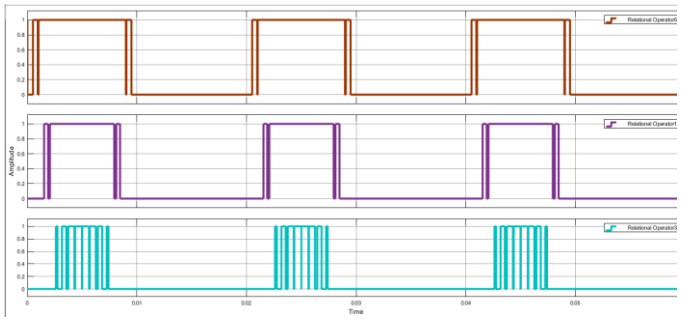
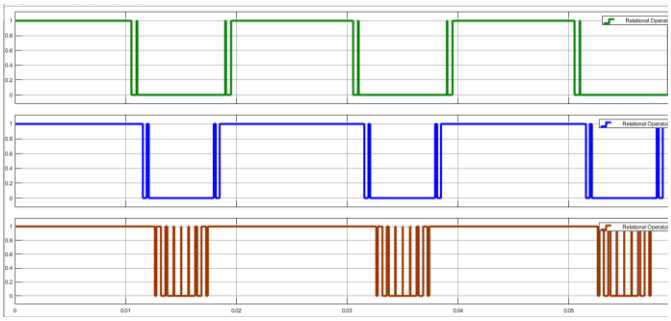


Fig.7. Alternate phase opposition disposition MCPWM.

The positive and negative output of relational operator signals for APOD MCPWM are shown in fig.8. (a) and (b).

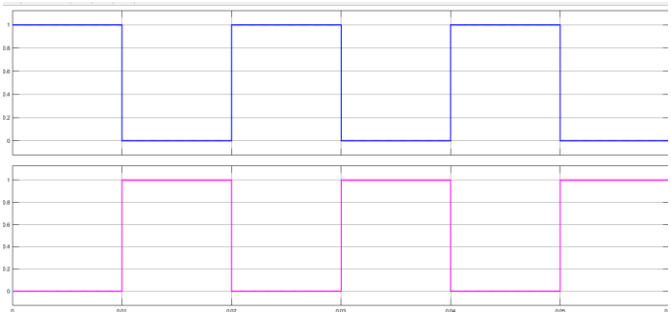


(a)



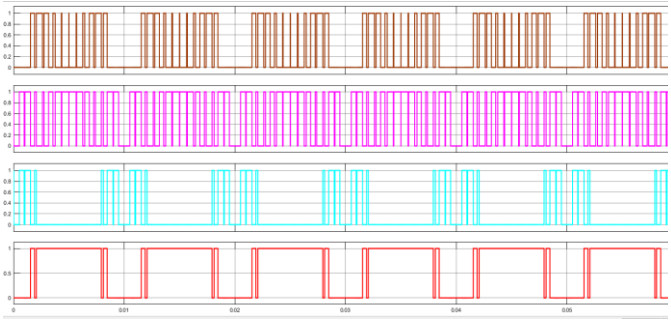
(b)

The Pulses for switches S_1, S_2, S_3, S_4, for half positive and half negative cycle of output voltage respectively are shown in fig.8. (c).



(c)

The pulses of switches from S5 to S8 for levels generation are shown in fig.8. (d).



(d)

Fig.8. Control signals of APOD MCPWM
(a)P_1, P_2, P_3, (b) N_1, N_2, N_3, (c) S_1, S_2, S_3, S_4, (d) S_5, S_6, S_7, S_8.

Output waveform of RDC CHBMLI contain 7-levels of voltage. Waveform is formed by three positive, three negatives, and a zero level.

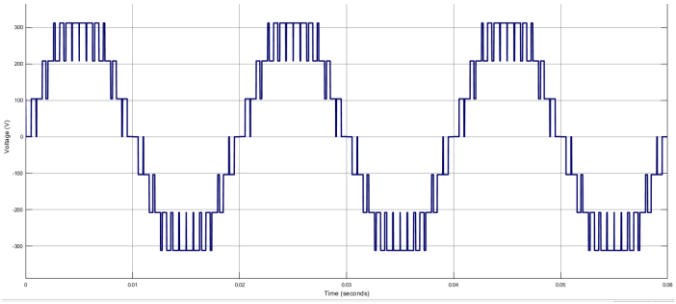


Fig.9. Output voltage waveform of proposed RDC-MLI implemented by APOD MCPWM.

V. CONCLUSION

The Seven-Level reduced device count cascaded H-Bridge multi-level inverter is developed on MATLAB-Simulink software. Designed RDC MLI consist of 8 semiconductors switches with 2 asymmetrical voltage sources. The multicarrier PWM techniques provide effective triggering to MLI. The level-shifted POD and APOD multicarrier PWM are implemented in RDC MLI. It is analyzed that RDC Cascaded H-Bridge with alternate phase opposition disposition MCPWM has better performance compared to POD MCPWM.

REFERENCES

[1] Korai, J. J., Mahar, M. A., Larik, A. S., Soomro, F. U. R., Ali, I., & Awan, M. S. (2020). Design Level Shifted Multicarrier Techniques for Cascaded H-Bridge Sub-Multilevel Inverter.

[2] Chappa, A., Gupta, S., Sahu, L. K., Gautam, S. P., & Gupta, K. K. (2019). Symmetrical and asymmetrical reduced device multilevel inverter topology. *IEEE Journal of Emerging and Selected Topics in Power Electronics*.

[3] Prabaharan, N., & Palanisamy, K. (2017). A comprehensive review on reduced switch multilevel inverter topologies, modulation techniques and applications. *Renewable and Sustainable Energy Reviews*, *76*, 1248-1282.

[4] bin Arif, M.S., Ayob, S.M. and Salam, Z., 2016, November. Asymmetrical multilevel inverter topology with reduced power semiconductor devices. In *2016 IEEE Industrial Electronics and Applications Conference (IEACon)* (pp. 20-25). IEEE.

[5] Gupta, S. K., & Bansal, P. (2018, October). Reduced Device Count Asymmetrical Multilevel Inverter Topology Using Different PWM Techniques. In *2018 2nd IEEE International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES)* (pp. 343-348). IEEE.

[6] Siddique, M. D., Mekhilef, S., Shah, N. M., & Memon, M. A. (2019). Optimal design of a new cascaded multilevel inverter topology with reduced switch count. *IEEE Access*, *7*, 24498-24510.

[7] Dasari, M. S., & Mani, V. (2020). Simulation and analysis of three-phase parallel inverter using multicarrier PWM control schemes. *SN Applied Sciences*, *2*(5), 1-10.

[8] Mustafa, İ. N. C. İ. (2019). Performance evaluation of multi-carrier PWM techniques: PD, POD and APOD. *International Journal of Applied Mathematics Electronics and Computers*, *7*(2), 38-43.

[9] Mahar, Mukhtiar Ahmed, Muhammad Aslam Uqaili, and Abdul Sattar Larik. "Harmonic analysis of ac-dc topologies and their impacts on power systems." *Mehran University Research Journal of Engineering & Technology* 30.1 (2011): 173-178.

[10] Nagarajan, R., & Saravanan, M. (2012). Performance Analysis of Multicarrier PWM Strategies for Cascaded Multilevel Inverter. *European Journal of Scientific Research*, *92*(4), 608-625.