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Development of Simulation Model for Seven Level Asymmetric Cascaded Half Bridge Multilevel Inverter

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***Abstract*—Renewable energy has made quite a mark in the world's growing energy demand. This form of energy is proven to be economical as well as environmental-friendly. This calls for the need of DC to AC power conversion, which is achieved by means of an inverter. Greater harmonic distortion, higher switching losses and poor power quality waveform were the main setbacks of former inverters, this created a path for the advent of multilevel inverters. In this paper, a 7-level asymmetric CHB-MLI has been modelled via MATLAB/SIMULINK software. In order to further reduce the THD and control the output, multicarrier PWM technique of phase opposition disposition has been implemented. THD for the proposed scheme has been calculated to be 16.24%. THD analysis has been carried out, using FFT analysis tool of MATLAB/SIMULINK. 7-level voltage output has been displayed. A comparison of various parameters of different topologies with the proposed topology has been accomplished.**

***Index Terms*— Cascaded H-Bridge, Multicarrier PWM technique, Multilevel Inverter, Phase Opposition Disposition (POD), Total Harmonic Distortion**

I. INTRODUCTION

Recent advancement in renewable energy production and consumption has revolutionized the energy sector. With this rapidly developing technology, the need and demand for efficient power conversion is at its peak. An inverter is an electronic device which transforms DC power to AC power, utilizing different combination of switches [1-3]. Conventionally, 2-level (square wave) and 3-level (quasi square wave) inverters were used for this purpose. Due to their poor-quality waveform and high harmonic content, they have been superseded with the invent of multilevel inverters (MLI) [4]. MLI produces multi-stepped waveform which is several times more efficient than the output of conventional inverters [5-7]. It has lower harmonic content, lesser switching losses and better-quality output waveform [8-10]. It has been implemented in various applications, such as motor drives, flexible AC transmission systems (FACTS), renewable energy interfacing, etc. due to its obvious advantages over traditional inverters [11][12].

The three basic MLI configurations are cascaded H-bridge (CHB) MLI, diode clamped (DC) MLI and flying capacitor (FC) MLI. The cascaded arrangement is further classified into asymmetric and symmetric arrangements. The asymmetric arrangement incorporates unequal DC sources in its H bridge, whereas symmetric uses equal DC sources. In order to control the output voltage waveform and further reduce the THD and switching losses, different modulation methods are implemented. The specific arrangement and modulation technique selection is dependent on the power requirement. Switching techniques are categorized into two kinds i.e. fundamental frequency switching and high frequency switching. Among all other techniques, pulse width modulation (PWM) is widely used. It is further divided into phase disposition (PD), phase opposition disposition (POD) and alternate phase opposition disposition (APOD) techniques. As shown in Fig. 1

This paper proposes a simulation model for seven level cascaded asymmetric half bridge MLI arrangement. The output voltage has been taken by utilizing phase opposition disposition technique. Review of different MLI topologies has been conducted. Comparison curves showing the flexibility and cost effectiveness of the proposed arrangement have been sketched. The output voltage waveform and THD analysis has been carried out.

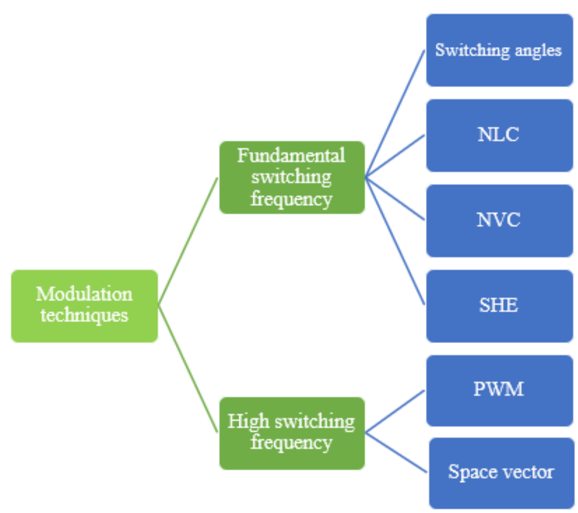

Fig. 1. Classification of Modulation Techniques

II. METHODLOGY

We have used MATLAB/SIMULINK software to develop the simulation model. FFT analysis tool is used to calculate the THD of output voltage.

For proposed model the model parameters are shown in Table I.

TABLE I: Model parameters.

Model Parameters	
Sine wave frequency	50 Hz
Switching frequency	1000 Hz
R	10 Ω
No. of Switches	8
No. of DC Sources	2
Output voltage levels	7
Magnitude of DC Sources	V1=12V
	V2=24V

III. EQUATIONS

In asymmetric cascaded H- bridge MLI, the magnitude of DC sources is obtained as;

$$V_{dc}, 2V_{dc}, 3V_{dc}, \ldots, pV_{dc}$$

Here,

$$V_1=V_{dc}$$

$$V_2=2V_1$$

$$V_3=3V_1$$

Hence,

$$V_p= pV_{dc} \qquad (1)$$

Where,

p shows the integral multiple of *V1*

Following equations (2) and (3) show the quantity of switches and output voltage levels respectively.

$$q= 2*p \qquad (2)$$

Where,

p denotes DC sources quantity.

The equation for number of voltage levels at output is given as:

$$= 2^{p+1} - 1 \qquad (3)$$

Where,

p denotes DC sources quantity.

IV. SIMULATION MODEL

The proposed simulation has been modelled in MATLAB/SIMULINK software, which is developed by MathWorks Inc. The POWERGUI tool has been used for THD and output voltage analysis.

A. Main Circuit

The simulation model comprises of eight MOSFETs in total, from which four are used for level generation and remaining four are used in polarity changer circuit. It incorporates two DC sources, of 12V and 24V, in each power cell. As seen in Fig. 2. Table II shows the storage parameters.

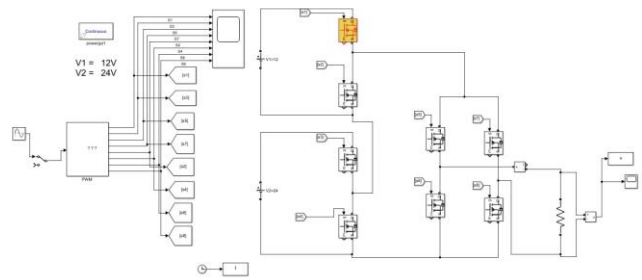

Fig. 2. Simulation Model for 7-level Asymmetric Half Bridge CHB MLI

B. Generalized Control Circuit

The control circuit comprises of several comparators to generate the multicarrier waveform with POD technique. It can be seen in Fig. 3. Multicarrier PWM is used to produce desired gating signals for switches. It is shown in Fig. 4. The respective pulses used to trigger the MOSFETs from s1 to s8 are shown in Fig. 5. The pulse width technique creates sufficient delay to trigger the switches accordingly to generate seven level voltage output wave-form.

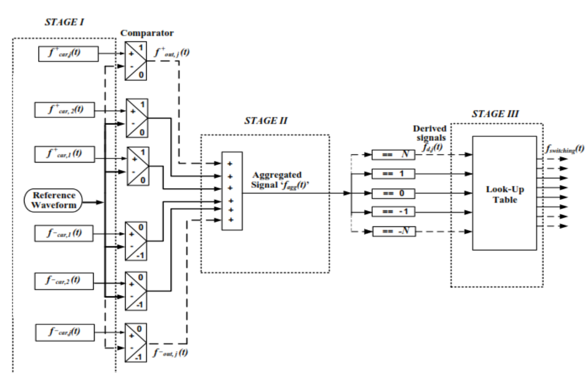

Fig. 3. Generalized Control Circuit for Asymmetric Half Bridge CHB MLI

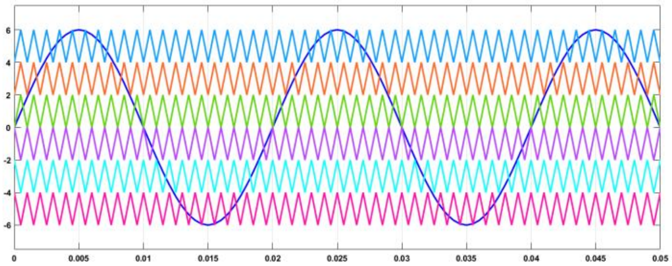

Fig. 4. Multicarrier PWM Signal

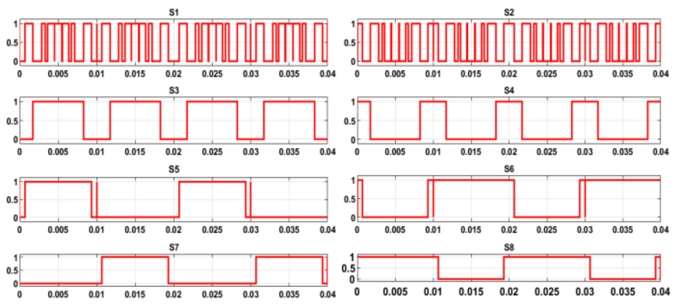

Fig. 5. PWM Signals to trigger switches s1 to s8

V. OPERATION OF MODEL

The proposed model for asymmetric half bridge CHB MLI comprises of eight MOSFETs, among which four are used in level generator and polarity changer circuit, which is shown in Fig. 6. To receive the 7-level stepped output, the switches are signaled using POD PWM technique, according to the switching pattern shown in TABLE II, the respective operation modes for the proposed model are shown in Fig. 7. In MODE 1, switches s1, s4, s5 and s8 are triggered to give the output V1. Similarly, different combinations of switches are used, based on proposed switching pattern, to give 7-level stepped output waveform.

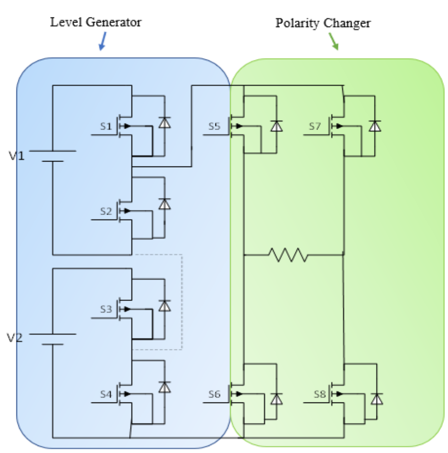

Fig. 6. PWM Signals to trigger switches s1 to s8

TABLE II: Switching Patterns.

	S1	S2	S3	S4	S5	S6	S7	S8	V_O
1	1	0	0	1	1	0	0	1	V1
2	0	1	1	0	1	0	0	1	V2
3	1	0	1	0	1	0	0	1	V1+V2
4	0	1	0	1	1	0	0	1	0V
5	1	0	0	1	0	1	1	0	-V1
6	0	1	1	0	0	1	1	0	-V2
7	1	0	1	0	0	1	1	0	-V1-V2

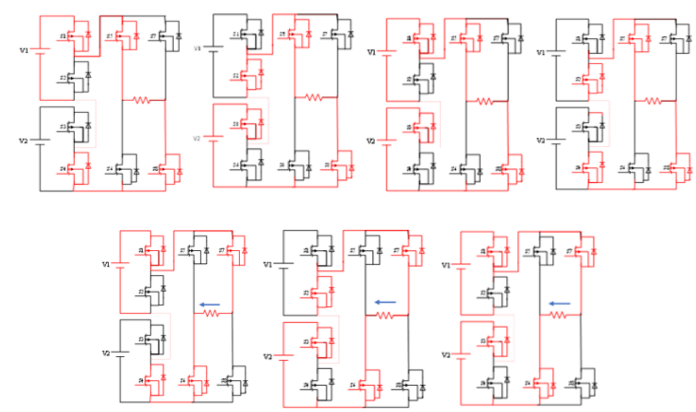

Fig. 7. Operation Modes from MODE 1 to MODE 7

VI. RESULTS

The 7-level output voltage waveform for asymmetric half bridge CHB-MLI is shown in Fig. 8. Each step has a difference of 12V. The total harmonic distortion (THD) is found to be 16.24%. The THD analysis was carried out using the FFT analysis tool of MATLAB/SIMULINK software. It is shown in Fig. 9.

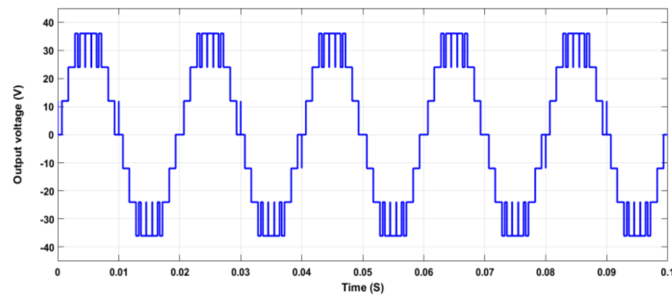

Fig. 8. Output Voltage Waveform

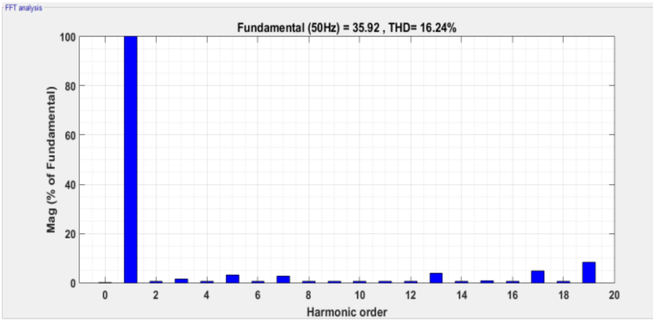

Fig. 9. THD of Output Voltage

VII. COMPARISON CURVES FOR DIFFERENT CONFIGURATIONS

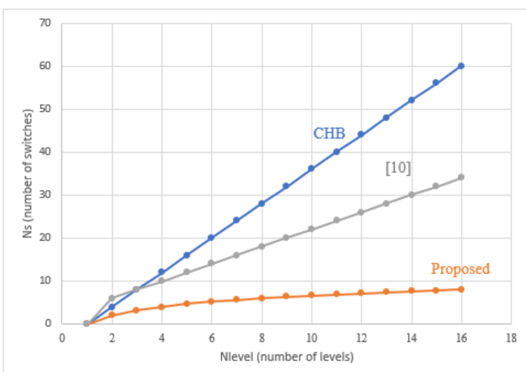

Fig. 5(a). Number of Sources vs Number of Levels

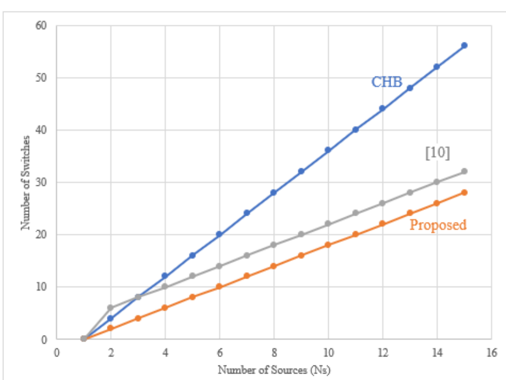

Fig. 5(b). Number of Sources vs Number of Switches

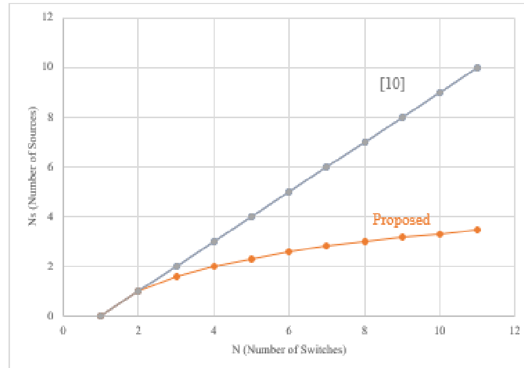

Fig. 5(c). Number of Switches vs Number of Sources

VIII. CONCLUSION

A simulation model of 7-level asymmetric cascaded H-bridge MLI has been modelled. The FFT analysis of output voltage waveform is carried out at 35.92 and THD is 16.24%.

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